Hall Ticket Number:

Code No. : 14648

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (I.T.) IV-Semester Main & Backlog Examinations, August-2022

Computer Organization

Time: 3 hours Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	List the different Special registers available in a CPU. Mention the purpose of each.	2	1	1	1
2.	Mention Four difference between SRAM & DRAM.	2	2	1	1
3.	A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. a. How many selection inputs are there in each multiplexer? b. What size of multiplexers are needed? c. How many multiplexers are there ill the bus?	2	3	2	2
4.	Design a 4-bit combinational circuit decrementer using four full-adder circuits.	2	2	2	2
5.	Mention various steps involved in data transfer from source to destination using Strobe pulse method.	2	1	3	1
6.	How many characters per second can be transferred over a 1200 baud line in the following modes? a) Synchronous serial transmission. b) Asynchronous serial transmission with two stop bits.	2	2	3	2
7.	How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?	2	3	4	2
8.	How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?	2	3	4	2
9.	Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.	2	1	5	1
10.	A nonpipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a dock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?	2	2	5	2

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	Part-B (5 × 8 = 40 Marks)				
11. a)	With an example explain the following addressing modes. a) Direct addressing b) Register Indirect addressing c) Auto Increment d) Relative addressing	4	2	1	1
b)	Evaluate the following equation using Two and Zero instruction formats. [(X + Y) / (P –Q) * R]	4	2	1	2
12. a)	Explain the difference between hardwired control and microprogrammed control. Is it possible to have a hardwired control associated with a control memory?	4	2	2	1
b)	Formulate a mapping procedure that provides eight consecutive microinstructions for each routine. The operation code has six bits and the control memory has 2048 words.	4	4	2	2
13. a)	What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each?	4	1	3	1
b)	A CPU with a 20-MHz clock is connected to a memory unit whose access time is 40 ns. Formulate a read and write timing diagrams using a READ strobe and a WRITE strobe. Include the address in the timing diagram.	4	3	3	2
14. a)	Criticize the following statement: "Using a faster processor chip results in a corresponding increase in performance of a computer even if the main memory speed remains the same."	3	4	4	2
b)	A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers. a. How many RAM and ROM chips are needed? b. Draw a memory-address map for the system. c. Give the address range in hexadecimal for RAM, ROM, and interface.	5	2	4	2
15. a)	Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching.	3	3	5	2
b)	A 05 stage pipeline has the stage delay of 150,120,160,140,100 n secs, respectively. Registers that are used between stages have a delay of 10 n secs each. Assuming a constant clock ratings, what is the total time taken by pipeline for 100 tasks?	5	3	5	2

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16. a)	What is the difference between High level, Assembly and Machine level languages? Classify the assembly language instructions according their function and give an example to each.	4	1	1	1
b)	What is the difference between a microprocessor and a microprogram? Is it possible to design a microprocessor without a microprogram? Are all microprogrammed computers also microprocessors?	4	1	2	2
17.	Answer any ***two*** of the following:				
a)	How data will be transferred in destination initiated Hand Shaking Method? Explain with proper diagram.	4	2	3	1
b)	A virtual memory system has an address space of 8K words, a memory space of 4K words, and page and block sizes of IK words. The following page reference changes occur during given time interval. (Only page changes are listed. if the same page is referenced again, it is not listed twice.) 4 2 0 1 2 6 1 4 0 1 0 2 3 5 7 Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used Is (a) FIFO; (b) LRU.	4	3	4	2
c)	Consider a computer with four floating-point pipeline processors. Suppose that each processor uses a cycle time of 40 ns. How long will it take to perform 400 floating-point operations? Is there is a difference lf the same 400operations are carried out using a single pipeline processor with a cycle time of 10 ns?	4	4	5	2

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	22.5%
ii)	Blooms Taxonomy Level – 2	36%
iii)	Blooms Taxonomy Level – 3 & 4	41.5%

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